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The paragraph beginning on line 6 of page 3 has been amended as follows:

Because the array 6 might be quite large, the number of signal lines 12 typically is considerably smaller than the number of column lines 16. Therefore, the signal lines 12 typically are used to sequentially access the SLM cells 20 K cells at a time (where "K" represents the number of signal lines and typically is less than the number (M) of columns) [at a time] by activating the appropriate transistors 18. Because only K bit lines 16 are driven with new values (and thus, only K transistors 18 are activated), the remaining column lines 16 are in a tri-state condition and are coupled to the nonselected capacitors 24 of the row. Therefore, charge sharing typically occurs between the capacitors 24 and the tri-stated column lines 16.